AMENDMENT TO THE SPECIFICATION

Please amend the Specification as follows:

Page 6, line 1 to page 6, line 21:

Fig. 1 is a functional block diagram of the QCEXO clock system 10. The system comprises four quad compensated clocks, of which only two are shown at 20A and 20B for clarity. Outputs QR1, QR2, QR3 and QR4 from all four quad compensated clocks are input into a digital signal processor (DSP) 24. These outputs are also input to a gate array 18, which selects which reference oscillator output, or combination of reference oscillator outputs, are uses as a clock source for the DSP 24. Output of the gate array 18 is input to a phase locked loop (PLL) 22 that converts the selected clock frequency or frequencies to a clock reference signal required by the DSP 24. The gate array 18 is controlled by feedback from the DSP 24. Output QT from a temperature sensing oscillator 16 is input to the DSP 24. The temperature sensing oscillator 16 also comprises a quad compensated resonator. The quad compensation methodology compensates the temperature measurement for adverse effects of acceleration, and improves the accuracy of the temperature measurement by using the averaged output of the four oscillator crystals in the array. The quad compensated temperature signal ~~OT~~ QT is used to make temperature related compensation in the QCEXO system, as will be discussed in detail in subsequent sections of this disclosure. Preferably, one oscillator crystal, comprising the quad compensated temperature resonator, is physically located in each of four quadrants and close proximity to a corresponding one of the four quad compensated clocks in the ensemble. The averaging of outputs of the four temperature oscillator crystals then yields an accurate representation of the average temperature exposure of the clock ensemble.